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DESIGN AND FABRICATION OF AN ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

FOURTH INTERIM PROGRESS REPORT

April 1967

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by

Westinghouse Research Laboratories
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SUMMARY

An analysis of the operational amplifier circuit has allowed a reduction in the number of active components. A review of the tantalum component work has been carried out and the possibility of utilizing tantalum nitride has been explored.

INTRODUCTION

The requirement for the project is an integrated circuit form of a circuit which converts a variable low power level dc signal to a digital output such that the digital output on time portion of the cycle is proportional to the dc input signal magnitude.

The previous interim progress report outlined the work involved in transferring the project to the Westinghouse Research Laboratories and indicated that a re-evaluation of the breadboard model was being carried out.

During this present period the design review was continued and the results of this work are reported. A thorough survey of the field of tantalum thin film technology was also carried out and the factors affecting the stability of tantalum components were reviewed. The possibility of employing tantalum nitride instead of the oxide was also considered. A summary of this literature survey is presented in Appendix 2.

THEORETICAL CIRCUIT CONSIDERATIONS

1. Analysis of Linearity Specification with Regard to Circuit Design

The ramp or triangular waveform generator of the voltage/duty cycle generator consists of an integrator operating on a square wave input. The overall linearity specification of 2.5% implies a ramp linearity of 2.5% or better.

The linearity of the ramp waveform v_o in Figure 1 is dependent on the behavior of the amplifier input voltage v_i and the capacitor current i_c, since

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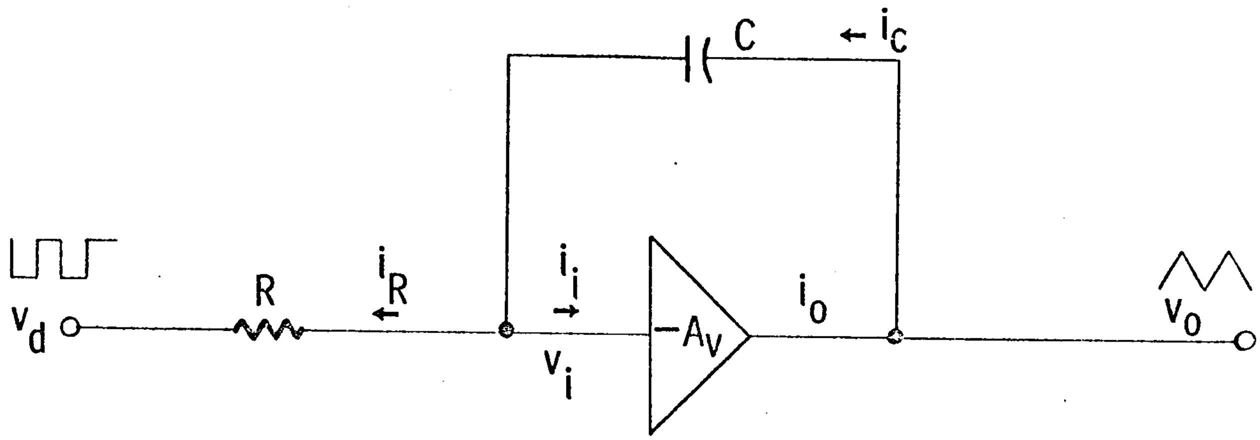

Fig. 1

4.

$$v_o = v_i + \int \frac{i_c}{c}\, dt. \tag{1}$$

As shown in Appendix 1, if the capacitor current i_c varies linearly with time, with an initial value I_o and a final value $I_o + \dot{I}t_o$, where $\dot{I}$ is constant and t_o is the ramp duration, then the current change $\dot{I}t_o$ may be as great as 20% of I_o and the waveform linearity still be 2.5%.

In light of this fact, the operational amplifier adopted for this application as of the First Interim Progress Report dated March 15, 1966, the essentials of which are shown in Figure 2, is far better than is needed for this requirement. To show this, consider from Figures 1 and 2,

$$\begin{aligned} i_c &= i_R + i_i \\ &= \frac{v_d - v_i}{R} + \left(\frac{i_o}{A_i} + \frac{v_o}{r_{21}} \right), \end{aligned} \tag{2}$$

where A is the current gain of the amplifier and r_{21} its transresistance, or $\left(\frac{\partial v_o}{\partial i_i} \right)_{io}$. In (2), $v_i = \frac{v_o}{A_v}$, where $A_v \approx 4000$ is the voltage gain of the amplifier, and the driving voltage v_d is a square waveform independent of v_o except at the ramp end points and is constant during the ramp, therefore the first term in (2) is $i_R = \frac{v_d - v_i}{R} = \frac{v_d}{R} - \frac{v_o}{RA_v}$, and $(\Delta i_R)_{max} = \frac{\Delta v_o}{RA_v} = \frac{4V}{1K \times 4 \times 10^{-3}} \approx 10^{-6}$ A. The second term of (2), i_i, includes two components. The first is $\frac{i_o}{A_i} \lessapprox \frac{i_o}{10^4}$, where $A_i = \bar{\beta}^4 = 10^4$ is a conservative estimate of the amplifier current gain made by assuming the low average current gain per stage, $\bar{\beta}$, of 10, for each of

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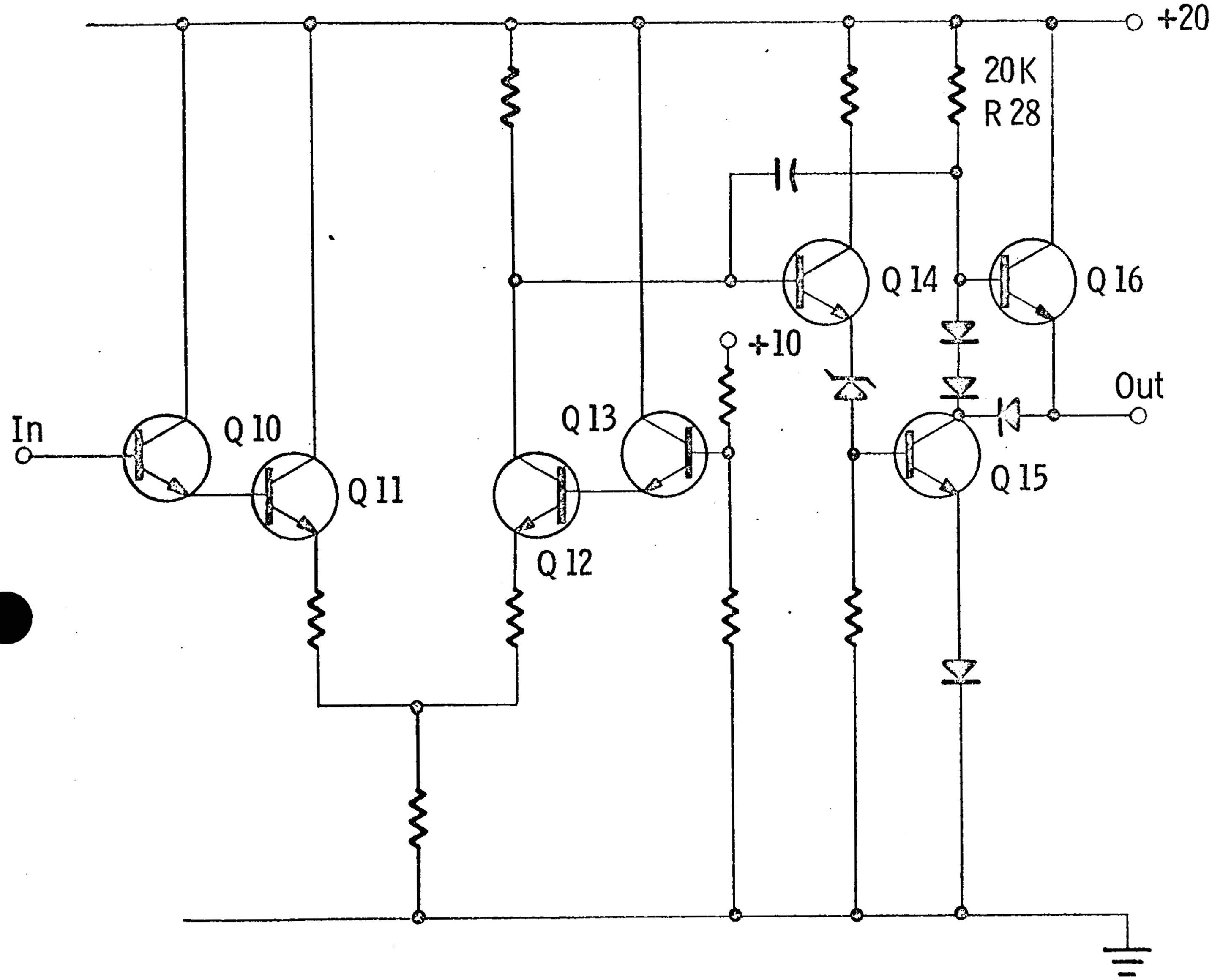

Fig. 2

the four stages in the amplifying chain. Since $i_o = i_c$ except at switching points, this cannot contribute to a change in i_c during the ramp.

The change in the second component of i_i is

$$\frac{\Delta v_o}{r_{21}} \simeq \frac{\Delta v_o}{R_{28} \times \overline{\beta}^{4}} \simeq \frac{4V}{8 \times 10^{10}} = 0.5 \times 10^{-10} \text{ A.}$$

Thus both terms on the right of (2) are negligible compared to the integrating current of $\pm \frac{2V}{1K} = \pm 2 \times 10^{-3}$ A.

In view of the foregoing, it appears reasonable to reduce the gain and hence complexity of the operational amplifier, or to reduce the integrating current employed in generating the ramp, or both.

Reducing the integrating current is especially desirable, since for the same operating frequency the integrating capacitor can be made smaller and hence easier to fabricate. This has been successfully accomplished and is further discussed elsewhere.

2. Analysis of Effect of Ramp Symmetry on Duty Cycle

When comparison of a triangular voltage waveform having fixed end points V_1 and V_2 with a dc voltage V_E (representing an error signal) is used to determine the switching times in the voltage/duty cycle generator, there is no effect on the duty cycle by the symmetry of the waveform. Thus, in Figure 3, the symmetric waveform v and the asymmetric waveform v^* are triangles having common base ($2t_o$) and height (V_2-V_1). The ON-durations of the switched waveforms are equal to the bases of the smaller, similar triangles with common height (V_2-V_E),

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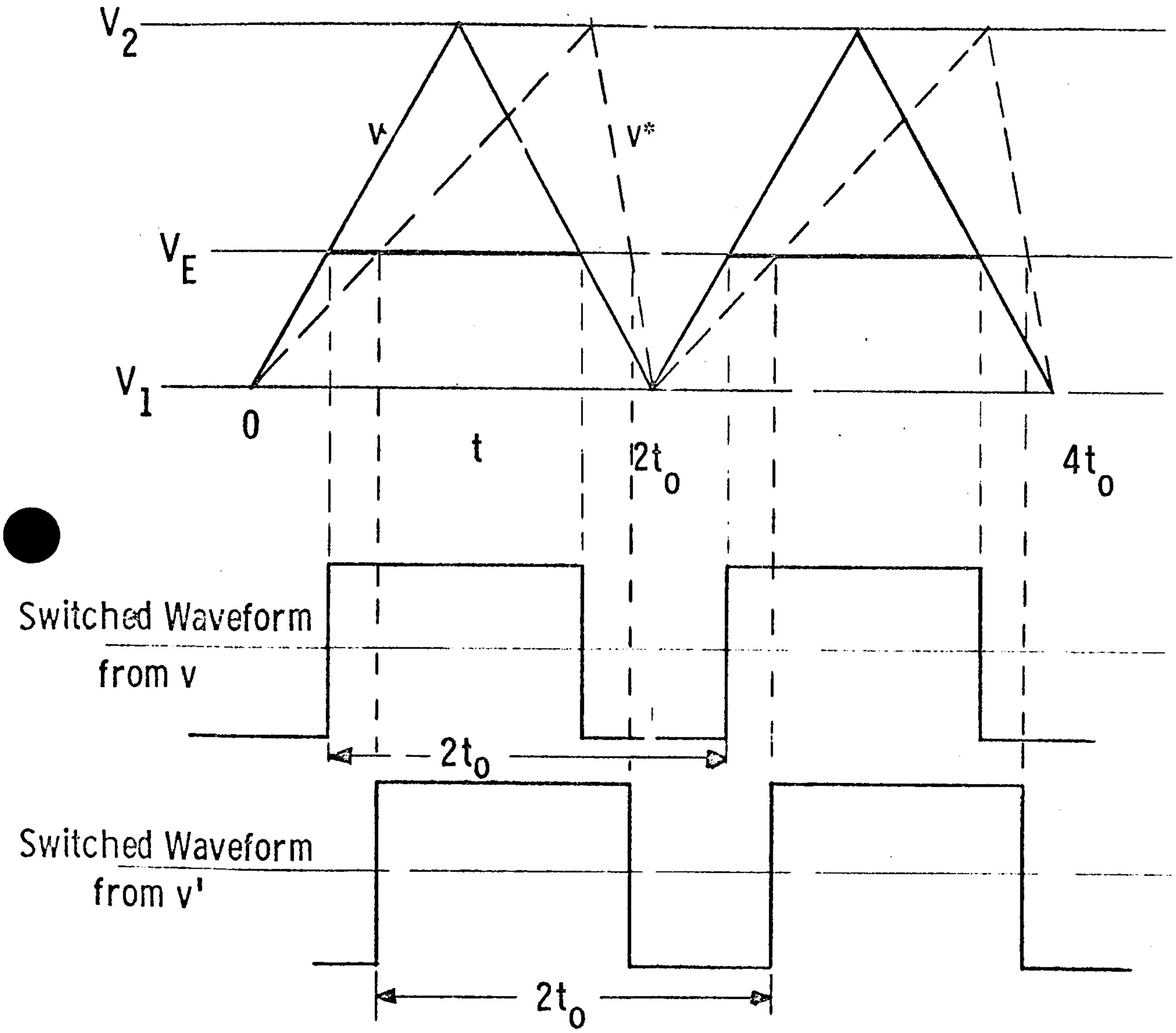

Fig. 3

consequently these bases must be equal, the ON-times must be equal, and hence the duty cycles must be equal for the two cases. Where the waveforms are slightly nonlinear, second-order effects may cause slight changes in duty cycle with symmetry, but in the present application they are entirely negligible.

It is important, however, that the switching points for changing from one output channel to the other be at the minima $t = 0$, $2t_o$ and $4t_o$ in Figure 3, when the power regulating transistors are in the OFF state, rather than at the maxima, or else a double frequency asymmetric output waveform will be generated.

Since the voltage/duty cycle generator is basically independent of triangular waveform symmetry, the operational amplifier in the waveform generator does not have to possess outstanding dc stability, which effects only the ratio of ascending slope to descending slope, but not end points or frequency. To take advantage of this fact, the amplifier shown in Figure 4 was constructed. It has roughly 2/3 the components of that in Figure 2 and has approximately the same voltage and current gain, but it has lower dc stability since it is single-ended throughout. Although it operated satisfactorily, it required stabilizing capacitors of 50 pf and 100 pf, which were considered too large for convenient fabrication, and so the design was not adopted.

A second simplification of the operational amplifier is that shown in Figure 5. This is also single-ended throughout, and is designed for lower voltage gain ($A_V \approx 200$) and current gain ($A_I \approx 4000$) than that of Figure 2, but should require no stabilizing capacitors.

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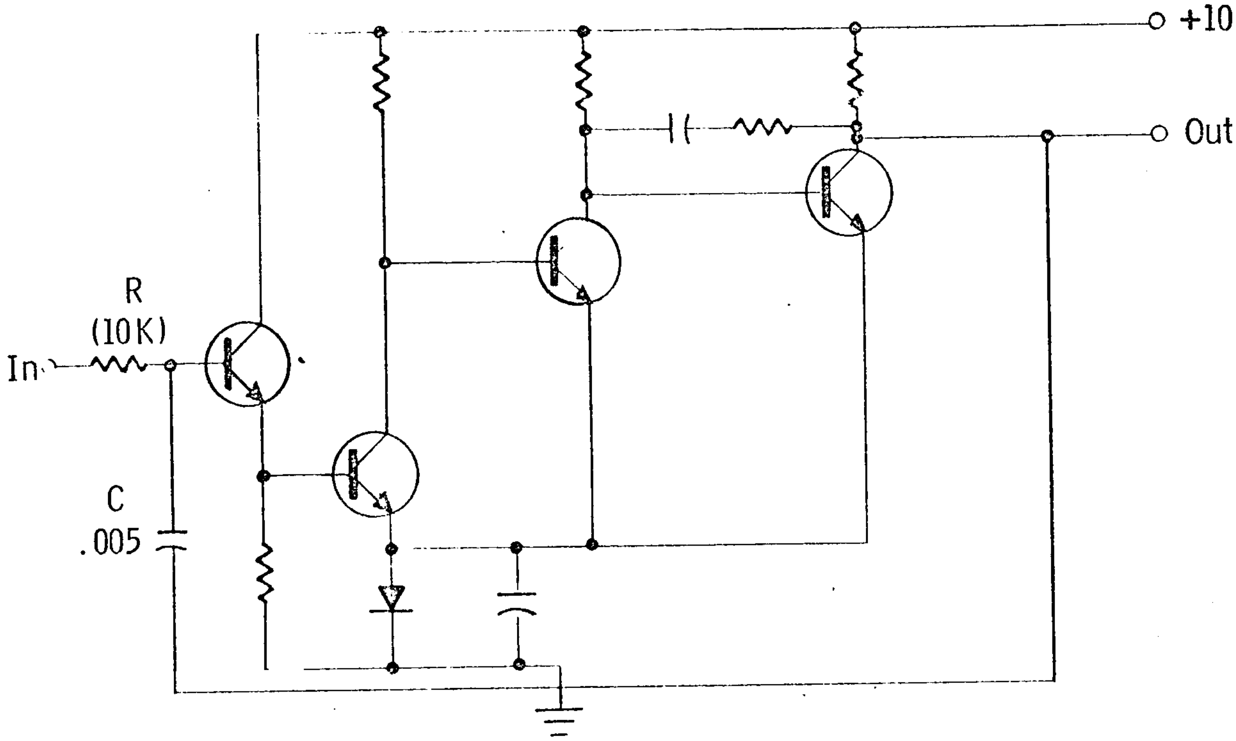

Fig. 4

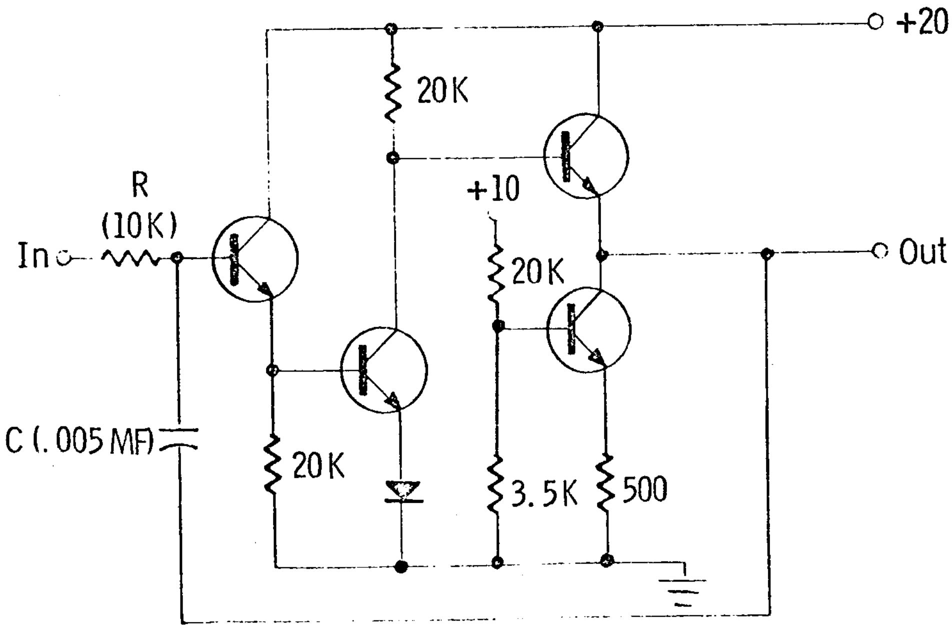

Fig. 5

It has less than half of the components in the circuit of Figure 2. It is expected to be more than satisfactory for the present requirement, but has not been built and tested as yet.

3. Analysis of Drive Requirements for the Integrator

Since the integrating current has been reduced, by a factor of 10, to $\pm \frac{2V}{10K} = \pm 2 \times 10^{-4}$ A through the use of an integrating capacitor and resistor having 10 times larger impedances, the need for the driving amplifier between the binary circuit and the integrator no longer exists. Tests of the circuit with this amplifier deleted show good performance, and therefore this change will be permanent. These tests are discussed elsewhere.

EXPERIMENTAL CIRCUIT WORK

The evaluation of the discrete component breadboard continued with a measurement of overall system linearity at 125°C over the full 100 mv input range. This measurement was made through the use of the time base of a 545 oscilloscope. The resulting data is shown in Table 1 and the corresponding curve is shown in Figure 6. Measurements were made for the condition for which the integrating capacitor was .0005 μf and the input resistor 100 KΩ. These values were adjusted slightly to set the operating frequency of the triangle generator at 2.5 kc.

The results of the high temperature measurement of system linearity as shown in Figure 6 indicate deviations to be less than the ± 2.5% specification.

An alternate design of the triangle generator was investigated in an attempt to reduce the fabrication requirements on the AVDC

Read	Calc.	Meas.	Dev.	Inp. Diff.	% (FS)
975	00.00	00.00	0.00	.04479	0.00
950	26.00	27.00	1.00		0.10
900	78.00	78.00	0.00	.03974	0.00
850	130.00	132.00	2.00	.03476	0.20
800	182.00	182.00	0.00	.02973	0.00
750	234.00	234.00	0.00	.02482	0.00
700	286.00	286.00	0.00	.01977	0.00
650	338.00	237.00	1.00	.01481	0.10
600	390.00	388.00	2.00	.00998	0.20
550	442.00	440.00	2.00	.00500	0.20
500	494.00	492.00	2.00	.00000	0.20
450	546.00	543.00	3.00	.00505	0.30
400	598.00	594.00	4.00	.00985	0.40
350	650.00	646.00	6.00	.01502	0.60
300	702.00	697.00	5.00	.01980	0.50
250	754.00	748.00	6.00	.02490	0.60
200	806.00	800.00	6.00	.02988	0.60
150	858.00	853.00	5.00	.03492	0.50
100	910.00	906.00	4.00	.03991	0.40
50	962.00	962.00	0.00	.04487	0.00
43	969.20	969.20	0.00	.04976	0.00

Discrete Component Breadboard

Results of Data Taken with .0005 µf
Capacitor and 100 KΩ Resistance at 125°C

Table 1

13

Curve 581237-B

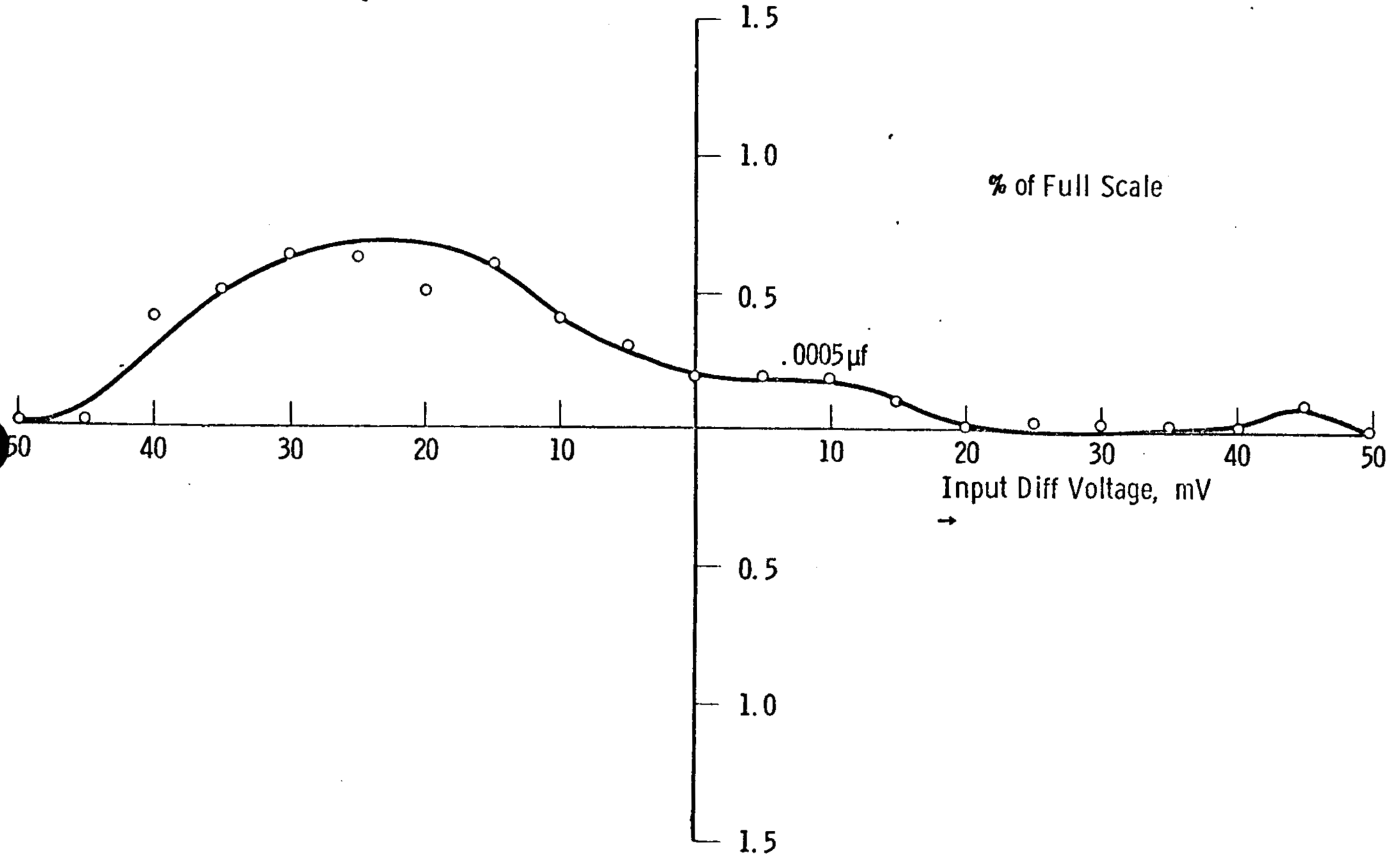

Fig. 6 — AVDC generator system linearity at 125°C

generator. The reduction in size of the integrating capacitor from a value of .05 μf to .005 μf permitted a simplification of both the bistable level detector and the operational amplifier. This simplification was possible due to the reduced current demand of the operational amplifier. The alternate design is shown in Figure 7 which shows the previous circuit of the operational amplifier reduced by one diode and one output transistor. In the same figure the bistable level detector is shown without the unity voltage gain driver eliminating the need for four transistors and five large value resistors.

System linearity measurements were made on this particular circuit arrangement at 125°C over the 100 mv input range. The data that was taken is shown in Table 2 and is shown plotted in Figure 8 . It can be seen that the nonlinearity is well within the "2.5% of full scale" specification set for the overall system.

A preliminary integrated circuit layout was initiated for the above design, however, this layout can be finalized only after the tantalum resistor and capacitor work is completed. Investigations must be made to determine a method of forming metal contacts from the integrated circuit to the capacitor. Also a means must be found for trimming the resistors and capacitors to the desired values. A problem arises also with the compatibility of tantalum with silicon dioxide since this oxide is attacked by the etches normally used to etch the tantalum.

As work progresses on the tantalum components, a number of the integrated circuit processes needed in the fabrication of this amplifier

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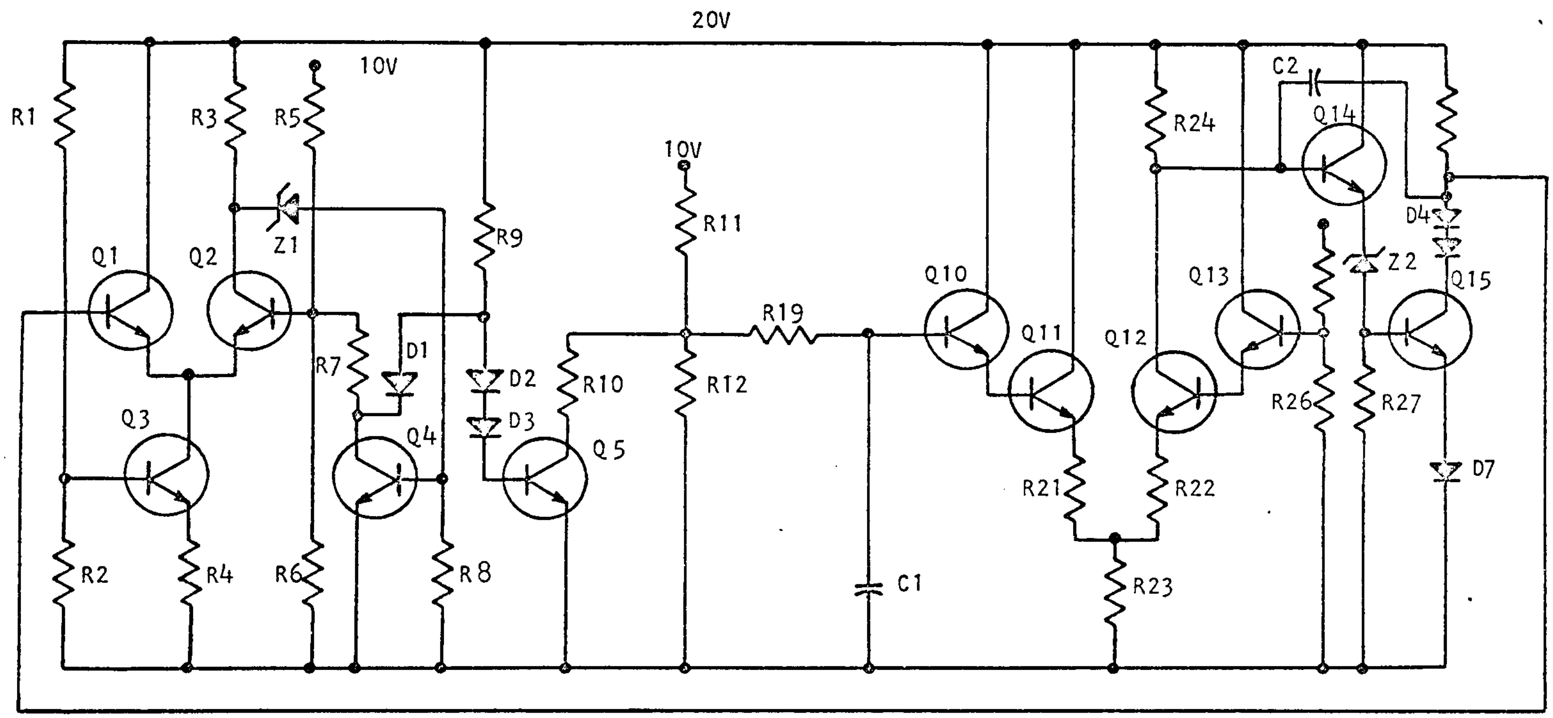

R1 = 9.1K	R9 = 20K	R24 = 20K
R2 = 1K	R10 = 1.5K	R25 = 5K
R3 = 13K	R11 = 3K	R26 = 5K
R4 = 1.3K	R12 = 7.5K	R27 = 10K
R5 = 3K	R19 = 10K	R28 = 7.5K
R6 = 7.5K	R21 = 510	C1 = .005
R7 = 1.5K	R22 = 510	C2 = 10pf
R8 = 6.8K	R23 = 3.0K	

Fig. 7

Read	Calc.	Meas.	Dev.	Inp. Diff.	% (FS)
950	00.00	00.00	0.00	.04479	0.00
900	47.29	43.00	4.29	.03974	0.42
850	94.59	90.5	4.09	.03476	0.40
800	141.88	136.0	5.88	.02973	0.59
750	189.18	183.2	5.98	.02482	0.60
700	236.47	230.5	5.97	.01977	0.60
650	283.77	282.1	1.67	.01481	0.17
600	331.06	324.2	6.86	.00998	0.69
550	378.30	371.1	7.20	.00500	0.72
500	425.65	418.5	7.15	.00000	0.72
450	472.95	465.0	7.95	.00505	0.79
400	520.24	511.9	8.34	.00985	0.83
350	567.54	556.5	11.0	.01502	1.10
300	614.83	601.4	13.4	.01980	1.34
250	662.13	648.6	13.5	.02490	1.35
200	709.42	694.8	14.6	.02988	1.46
150	756.72	743.7	13.0	.03492	1.30
100	804.01	795.5	8.51	.03991	0.85
50	851.31	846.5	5.80	.04487	0.58
25	875.00	875.0	0.00	.04976	0.00

Linearity Calibration of JPL Breadboard at 125°C

Alternate Design .005 μf Capacitor 10 KΩ Resistor

Table 2

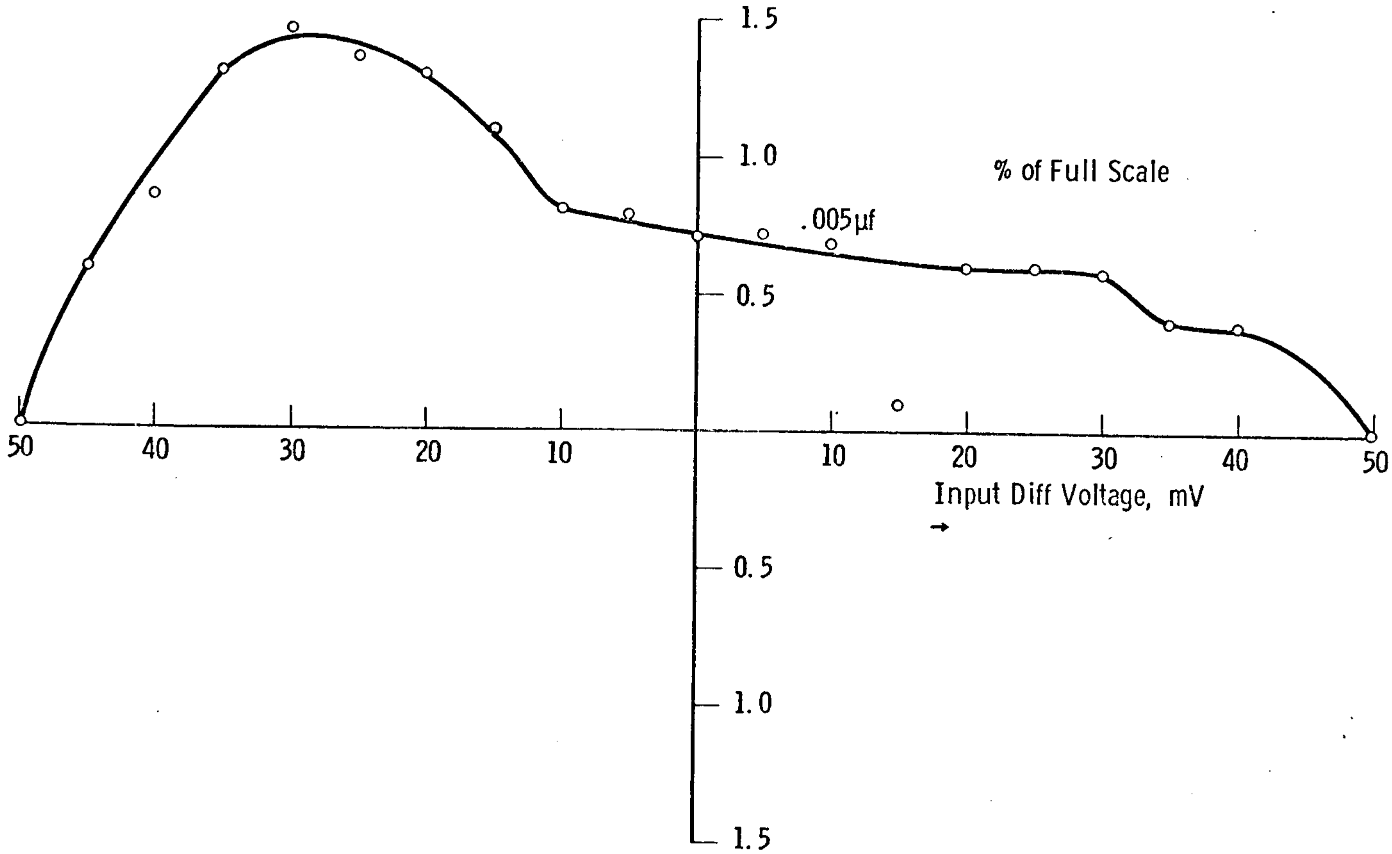

Fig. 8 —Alternate design AVDC generator system linearity

are being recycled and calibrated. This is true of both the "floating collector" epitaxial process and the insulating and surface passivation procedures and facilities.

PLANS FOR THE NEXT REPORTING PERIOD

Work on circuit optimization considerations will be continued. Tantalum components will be evaluated and the problems of tantalum component-silicon integrated circuit lead compatibility will be investigated.

APPENDIX 1

Linearity of a Voltage Ramp with Constantly Increasing Slope

If a voltage waveform has the slope given by

$$v = \int_0^t \frac{I_o + \dot{I}t}{C}\, dt \, ,$$

where $\dot{I}$ is a constant, then

$$v = (2I_o + \dot{I}t)\,\frac{t}{2C} \, , \text{ and at period } t_o ,$$

$$v_o = (2I_o + \dot{I}t_o)\,\frac{t_o}{2C} \, .$$

The straight line ramp having the same end points is

$$v' = v_o \frac{t}{t_o} = (2I_o + \dot{I}t_o)\,\frac{t}{2C} \, ,$$

and is shown in the accompanying figure. A 1

Hence, the linearity of the ramp is

$$\frac{(v'-v)}{v_o} = \frac{\dot{I}(t_o - t)\,\frac{t}{2C}}{(2I_o + \dot{I}t_o)\frac{t_o}{2C}} = \frac{t}{t_o}\,\frac{\dot{I}(t_o - t)}{(2I_o + \dot{I}t_o)}$$

This becomes maximum at

$$\frac{d}{dt}\left(\frac{v'-v}{v_o}\right) = 0, \text{ i.e., at}$$

$$\frac{\dot{I}(t_o - 2t)}{t_o(2I_o + \dot{I}t_o)} = 0, \text{ or at } t = \frac{t_o}{2} \, ,$$

and its value is

$$\text{LINEARITY} = \left(\frac{v'-v}{v_o}\right)_{max} = \frac{1}{2}\,\frac{\dot{I}\,\frac{t_o}{2}}{2I_o + \dot{I}t_o} = \frac{1}{8}\,\frac{\dot{I}t_o}{I_o}\left(\frac{1}{1 + \frac{\dot{I}t_o}{2I_o}}\right).$$

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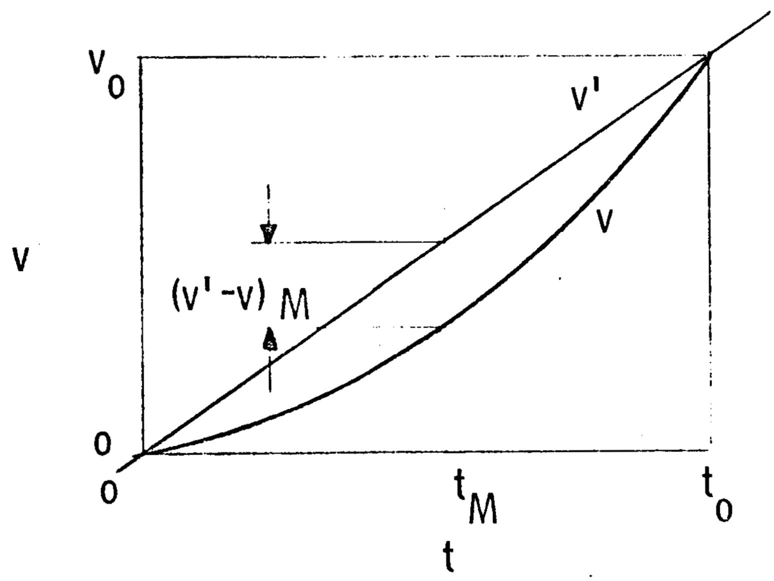

Fig. A1

If $\dot{I}t_o << I_o$, then

$$\text{LINEARITY} \simeq \frac{1}{8}\,\frac{\dot{I}t_o}{I_o}\,.$$

In other words, a voltage ramp waveform produced by integrating a constant current I_o plus a steadily increasing current component $\dot{I}t$, where $\dot{I}$ is constant, may satisfy a linearity specification if

$$\dot{I}t_o \leqslant 8 \times (\text{LINEARITY}) \times I_o.$$

If, as in the JPL voltage/duty cycle generator, LINEARITY = 2.5%, then the maximum allowable change of current $\dot{I}t_o$, and hence of ramp slope, is 8 x 2.5% = 20%.

APPENDIX 2

On the Properties of Thin Film Tantalum
Capacitors and Resistors

In order to prepare samples for desired values of resistance and capacitance, Gerstenberg, Mayer, Berry et al[3][5] indicate that the following information should be known:

(1) film thickness

(2) specific resistivity

(3) film depletion constant during anodization

(4) nitrogen concentration in the sputtering gas

(5) voltage potential between cathode and anode

(6) sputtering current

(7) sputtering rate (Å/sec or Å/min)

Gerstenberg and Mayer provide plots on page 59 (reference #5) which show that the use of nitrogen partial pressures between 0.03 and 1×10^{-3} torr results in significantly reproducible results in resistivity and temperature coefficients of the film.[6] Since the presence of other gases can suppress the formation of a stable tantalum nitride compound, it is necessary that the initial film be pure tantalum with a specific resistivity of less than 75 $\mu\Omega$ cm in order to attain reproducible properties.[5]

After the information required in the list above is obtained, the tantalum (or TaN) may be etched into resistor and capacitor patterns. This process is complete by covering the tantalum surface with a photosensitive emulsion over desired areas.[9][13] KPR and KMER have been reported for use with Au-Ta films[12] while a Kodak resist is reported when used with a HF, HNO_3 electrolyte. The etching solution to be used will be a one part HR, one part HNO_3 and two part H_2O solution at room temperature.[14]

Hass[7] has stated that photo-etched resistors are obtainable with a line width and spacing down to 1.5 mil.

The next step is the anodization of the films. The electrolyte is an agitated bath of 0.01% by weight H_2SO_4[14] at room temperature.

Some method will have to be devised whereby contacts on the resistors and capacitors can be made so that electrical measurements can be made.

Anodization occurs at different rates for tantalum and tantalum nitride. Since the capacitors cannot have a "trimming-up" anodization, these differences will have to be taken into consideration. McLean[9] reports that, for 0.01 μf Ta capacitors, anodization took place at 130 volts and 25°C. His discussion of the anodization of TaN should be considered before a decision in or out of favor is made. (See page 1455 of reference 9). Berry and Sloan[4] report that for tantalum film electrodes,with a thickness of 5000 Å and 250 mils in diameter, anodization voltages were found to be inversely proportional to the resulting capacitance. Their results are given as

Forming Voltage	Capacitance ($\mu\mu f$)
5	250,000
10	180,000
20	92,000
40	68,000
100	30,000
150	20,000
200	15,000

As far as the capacitors are concerned, one detail remains: the counter electrode. Both Au and Al have been used by Berry, Sloan, and Sikina and no differences in properties were observed between the two counter electrode materials. However, McLean[9] states:

> "Leakage and breakdown properties of tantalum film capacitors are dependent upon the top electrode material, as illustrated below. The metals at the top of the table form loosely adhering layers whereas those near the end adhere tenaciously and may introduce strain into the dielectric layer. Furthermore, as pointed out by Silcox and Maissel from studies of a somewhat different family of electrodes, the materials giving high breakdown voltages are ones that tend to agglomerate and it is unlikely that they will form continuous conductive paths through fissures and pores in the film."[9][14]

Effect of Counterelectrode on Anodic and Cathodic Breakdown Voltages

(0.035 μf Ta_2O_5 capacitors anodized to 100 volts, 105°C)

Metal	Deposition	Anodic BDV (Volts)
Au	Evap.	91
Pd	Evap.	90
Cu	Evap.	80
Sb	Evap.	75
Cd	Evap.	71
Fe	Evap.	45
In	Evap.	41
Al	Evap.	24
Ta	Sputtered	15

For these reasons it is suggested that copper or gold be used for a counter electrode.

The next step in the process is to thermally stabilize the resistors and capacitors by heating in an oven at 250 to 400°C and from 3 to 10% at 400°C.[6] All of the reference sources were in agreement with this step. The heating process causes the materials to age. If any changes are going to occur, they would take place then.

The resistors require one last anodization in order to obtain the exact value required. Haas[7] states that tantalum nitride films form anodic tantalum oxynitride on the surface which grows gradually with a very uniform thickness. The reduction in resistor thickness is 4 to 4.5 Å/volt and can be controlled to about .5 Å.[7] Gerstenberg[5] reports that anodizing of TaN films in 0.02% citric acid at 30 to 75 volts gave a film thickness decrease of about 4 Å/volt. A decrease for the Ta films was 7.5 Å/volt. McLean[9] reports oxide thicknesses of 16 Å/volt at room temperature and when a one hour period of soak at the anodizing voltage is included. Sikina[12] reports oxide growths of 25 Å/volt for Ta films.[14]

"Using automatic monitoring equipment, routine trimming of individual resistors is possible to 0.1%. By using very low current densities during anodization, a precision of ± 0.02% is attainable. Mass trimming of many resistors on a single substrate, while monitoring only one, is limited by the original uniformity of the film and the pattern geometry to about ± 3%."[7]

Several references [(3),(9),(12)] give details on life tests. Also general values and relationships for characteristics of TaN resistors and Ta_2O_5 capacitors have been obtained from the literature.

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